8.3 A 2.5Gb/s/pin 256Mb GDDR3 SDRAM with Series Pipelined CAS Latency Control and Dual-Loop Digital DLL

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As the range of applications for high-performance graphics and multimedia spread, the need for high-data-rate low-power graphics memory increases. In this work, the data rate of 2.5Gb/s/pin at a V_{DD} of 1.7v is achieved using GDDR3-based interface technology. The focus of this work is on several obstacles and solutions to achieve such performance. Areas investigated are the CAS-latency control, output control, and reducing DLL jitter to avoid data eye closing. The proposed circuits are fabricated on a 0.10μm dual gate-oxide DRAM process.

To achieve stable CAS latency (CL) at high frequency, the clock-domain-crossing delay, defined as the delay between the external clock domain and the DLL clock domain, needs to be compensated. A read command is generated after tCMD from the external CLK, and the DLL clock is generated at –tDO from the external CLK, where tDO is the delay between the DLL clock in the latency-control block and the DLL clock in the data-output block near the I/O pads. Therefore, the difference between the issue of read command and the DLL clock is tCMD+tDO, and it should be compensated in latency-control block. For compensation, delay-chain method (series pipeline) and FIFO method (parallel pipeline) [1] have been proposed. But it is difficult in the series pipeline to control each delay chain to have identical delay since each chain delay tND should be equal to (tCMD+tDO)/(CL–2).

In this work, the biased delay-chain method, shown in Fig. 8.3.1, is proposed. It uses identical biased inverters in every delay chain, so that each delay chain has the same number of inverters, and hence the same delay. The subchain delay is controlled through a register-programmed internal bias voltage. This voltage-controlled delay line (VCDL) method is shown in Fig. 8.3.2. A clock-deskew logic is used in the delay chains, because clock-skew integration, occurred by inconsistency of multiple chains, degrade the frequency limitation. Every biased inverter chain has dummy buffers or real buffers in order to operate as shift registers, so that all the inverter chains have the same loading, and skew is reduced as low as several tens of pico-seconds. For low-V_{DD} operation, no series PMOS is used in the subchain, because R_{on} resistance of MOS is inversely proportional to $V_{DD}–V_{th}$ and the body effect of V_{th} degrades the delay. In the conventional delay chain, the inverter has voltage dependency and does not include a method to test its real timing margin. The VCDL can solve these problems, because voltage-independent bias can overcome supply-voltage variation and the register control of the bias level makes it easy to test.

The data-output control is designed using the FIFO method (wave pipeline); which has the best access time in the SDRAM [2]. Two improvements are made to the conventional 4b-to-1b serialization: 2b serialization with half-clock shift, and 1b serialization using a tri-state buffer multiplexer, as shown in Fig. 8.3.3. The data_r1b and data_f1b are the same data as the last part of rdo and fdo, which are generated when routp1 and foutp1 are high. The 2b data is shifted before latched by foutp0 and routp1 pulse, and has broader timing margin of 1tCK. The tri-state inverter for 1b serialization has no clock coupling because of the series NMOS cascode stage. It also has no data feedthrough since data is applied to the inverter gate. In addition, low-V_{DD} margin is improved since there is no series PMOS. These advantages cause less jitter of the predriver node up/down that makes direct impact on the data eye. The data rdo, fdo are 0.5 tCK ahead of the clock rclkdo, fclkdo to allow for data-setup margin.

The ADDLL, shown in Fig. 8.3.4, features phase-detection dual-loop control, and enhanced duty-cycle correction (DCC). In the previous dual-loop system [3], the DCC period increases after locking state, so that jitter can be generated due to the alignment mismatch of rclk and fclk. The reason for the increased period is that the interpolation point of rclk and fclk (0.5tCK difference of rclk) is increased by supply-voltage variation. Figure 8.3.4 shows the circuits for the phase-detection dual-loop control system. The initial compensation-loop signal is determined by the majority voter with comparing the phase of rclk and fclk. Assuming that the value determined by the phase detector is clearly high in some period due to a large external voltage fluctuation or internal IR drop, dcc_invalid signal is high. Then, the dcc_invalid signal goes high and the control-loop selection is determined by pd_out, thus, the locking point is not changed. In this case, phase resolution is improved up to 0.5× tFDU (fine-delay unit), and there is no degradation of DCC performance. This is because the DLL always maintains alignment of the rising edges of rclk and fclk. During instant supply-voltage fluctuations, the value determined by phase detector is not clear, therefore, dcc_invalid is low. With the MUX select en_pre as compensation-loop signal, processing XOR with /UP, delay compensation information, the other delay-compensation loop is selected. The operation at this time is determined by the change of the previous compensation signal and the previous loop-delay information.

In the enhanced DCC with digital phase mixer, shown in Fig. 8.3.5, 2×N parallel sets of equal-sized tri-state inverter are used to mix the phases of the rising clock and the falling clock. In the conventional design, there is a trade-off between interpolation capability and operation frequency due to the inverter fan-out. In the enhanced DCC phase mixer, a two-stage mixer is adopted to improve both the operation frequency and the DCC capability. The first stage is the main DCC for duty –cycle correction. The second stage is the add-on DCC, acting as duty-cycle correction accelerator and controlled by registers to change the duty-cycle correction ratio for correcting the CLK distortion of various application systems. Figure 8.3.5 shows the comparison of DCC performances by output duty-cycle error versus input duty-cycle error. Experimental results show that DCC can correct less than ±2% of external-clock duty-cycle error of 12% (tCK=1.2ns).

This chip uses flip-chip package to reduce the inductance parasitic that could lead to power and ground noise. Data-input valid window is also improved by adopting wide bandwidth two-stage amplifier as a receiver. The shmoo plot at room temperature is shown in Fig. 8.3.6. The micrograph of the 9.25×7.70mm² 256Mb GDDR3 is shown in Fig. 8.3.7.

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References:
[1] S. B. Lee, et al. "A 1.6Gb/s/pin Double-Data-Rate SDRAM with Wave-Pipelined CAS Latency Control," *ISSCC Dig. Tech. Papers*, pp 210-212, Feb., 2004.
[2] H.J. Yoo, "A Study of Pipeline Architectures for High-Speed Synchronous DRAM's," *IEEE J. Solid-State Circuits*, vol. 32, no. 10, pp. 1597-1603, Oct., 1997.
[3] J.T. Kwak, et al. "A Low Cost High Performance Register-Controlled Digital DLL for 1Gbps ×32 DDR SDRAM," *Symp. VLSI Circuits,* pp. 283-284, Jun., 2003.

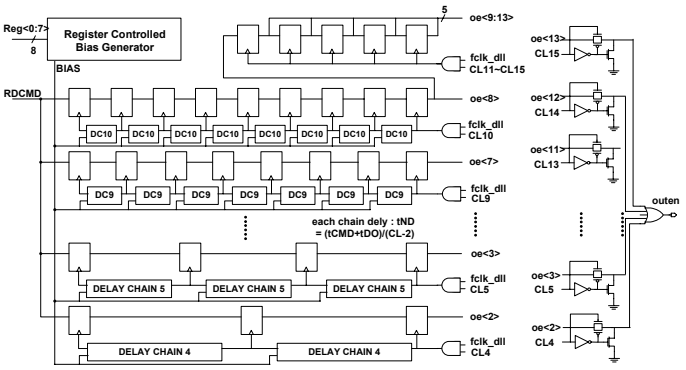

Figure 8.3.1: Series pipelined CAS-latency control circuit.

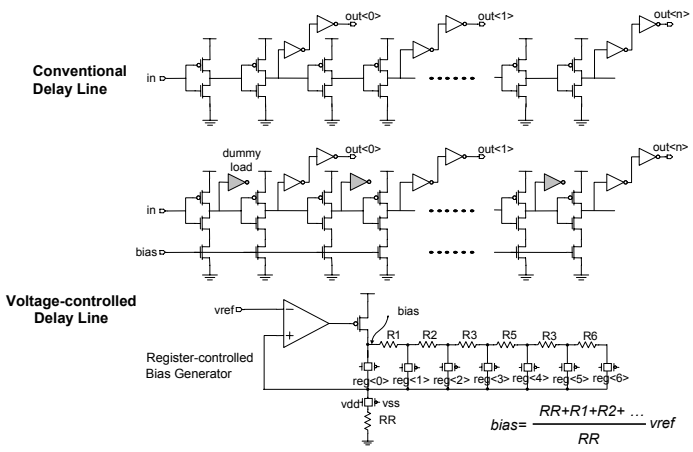

Figure 8.3.2: Voltage-controlled delay line (VCDL).

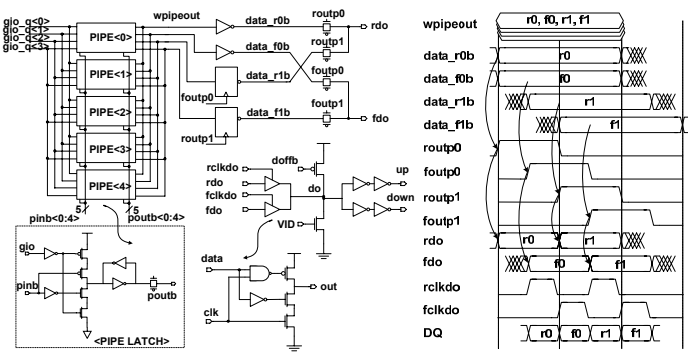

Figure 8.3.3: Wave pipeline latch and output serializer.

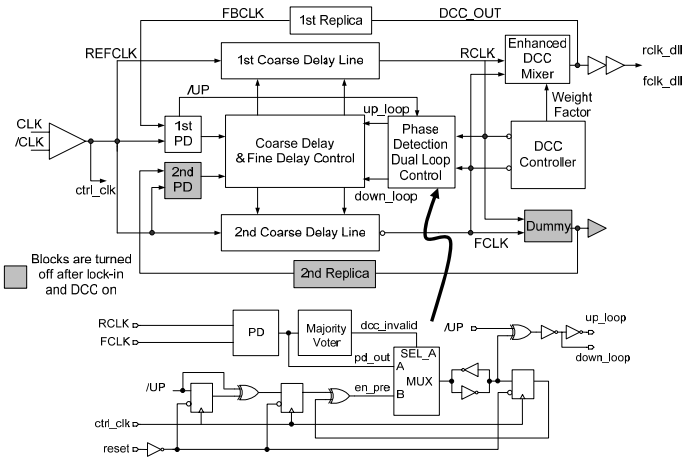

Figure 8.3.4: ADDLL with phase-detection dual-loop control.

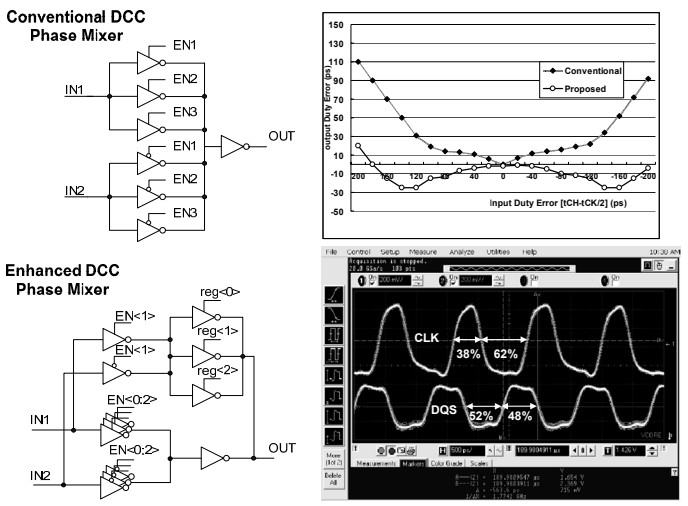

Figure 8.3.5: Enhanced DCC phase mixer.

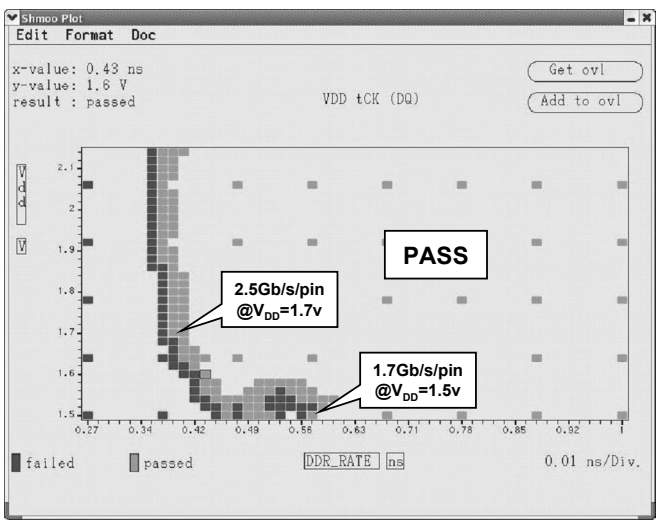

Figure 8.3.6: SHMOO plot of tCK versus V_{DD} at 25°C (full cell, all DQ)

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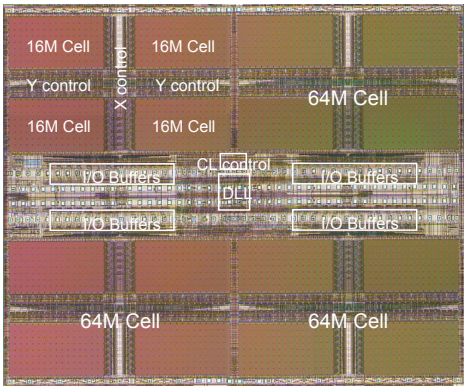

	Specification
Process	0.10μm 2M DRAM with dual gate-oxide
Chip Size	9.25mm x 7.70mm
Organization	4 bank (32 I/O) 136ball (package)
Refresh	4k / 32ms
Operation Voltage	1.5V ~ 2.5V
Max Data Rate	2.5Gb/s(@CL11)
tAA/tRCD/tRP	7.6ns / 7.3ns / 6ns (@ V_{DD}=1.7V)
tDS/tDH tIS/tIH	100ps / 100ps 50ps / 50ps
tAC/tDQSQ	250ps / 120ps
IDD2P (standby current)	50mA (tCK=1.0ns, V_{DD}=2.0V)

Figure 8.3.7: Micrograph of 256Mb GDDR3 SDRAM.

